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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,145	09/23/2003	Ellis Lee	TKHR6110-D1	7337

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EXAMINER
LEE, HSIEN MING

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,145	LEE ET AL.	
	Examiner	Art Unit	
	Hsien-ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-32,72,73 and 75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-32,72,73 and 75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The corrected drawing(s) filed on *9/10/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

HSIEN-MING LEE
PRIMARY EXAMINER

11/17/04

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. The objection and rejection, as set forth in the previous Office Action, are withdrawn.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 30 and 31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In re claim 30, the limitation "higher than a level of an interface between the first level air gaps and the first dielectric layer corresponding to a level between the conductive structure and the substrate" is not clear to the Examiner. In the specification, it does not provide any detail written explanation as to the foregoing limitation.

In re claim 31, the limitation " a height of an interface between the first level air gaps and the substrate is lower than a height of an interface between the conductive structure and the substrate" is not clear to the Examiner. In the specification, it does not provide any detail written explanation as to the foregoing limitation.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

> international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 17-20, 22, 24-25, 28, 72, 73 and 75 are rejected under 35 U.S.C. 102(e) as being anticipated by Bothra et al. (US 6,387,797).

In re claims 17-18, 24-25, Bothra et al., in Figs.2B-2E and related text, teach the claimed semiconductor interconnect structure, comprising:

- a conductive structure 206 (i.e. copper or aluminum or tungsten or polysilicon, col. 3, lines 13-14) having a top surface and a side surface;
- a first dielectric layer 210 over the conductive structure 206, having a first level air gaps 216 therein, wherein the side surface of the conductive structure 206 is surrounded by the first level air gaps 216 and an upper portion of the side surface is surrounded by the first dielectric layer 210;
- an etch stop layer 220 (i.e. silicon nitride or silicon carbide, col. 4, lines 39-41) over the first dielectric layer 210, wherein the etch stop layer 220 is disposed over the first level air gaps 216; and
- an opening 224 disposed over the top surface of the conductive structure 206 and part of the upper portion of the side surface of the conductive structure 206,wherein the first level air gaps 216 are isolated from the opening 224 by the etch stop layer 220.

In re claims 19-20, Bothra et al. also teach that the material of the first dielectric layer 210 and the etch stop layer 220 or 218 are different because the etch stop layer 220 or 218 has a high etch selectivity with respect to the first dielectric layer 210 (col. 3, lines 32-34).

In re claim 22, Bothra et al. also teach that the first dielectric layer 210 is doped oxide, i.e. fluorine-doped oxide or FSG (col. 4, lines 26-29).

In e claim 28, Bothra et al. further teach comprising a second dielectric layer 222 disposed over the first dielectric layer 210 and the etch stop layer 220, wherein the opening 224 exposes the conductive structure 206 through the first dielectric layer 210 and the second dielectric layer 222 (Fig.2E).

In re claims 72 and 75, Bothra et al. teach the claimed semiconductor interconnect structure, comprising:

* a substrate 202/204;

* a pair of conductive structures 206 and 208, wherein an air gaps 216 is disposed between the conductive structures 206 and 208; and

* a dielectric layer 210 over the conductive structures 206 and 208, the dielectric layer 210 having an etch stop layer 220 disposed over the air gap 216, wherein the dielectric layer 210 has an opening 224 disposed over at least a portion of the conductive structures 206 and at least a top portion of the etch stop layer 220, the opening 224 being isolated form the air gap 216.

In re claim 73, Bothra et al further teach that the etching selectivity of the dielectric layer 210 with respect to the etch stop layer 220 is substantially high (col. 3, lines 56-61).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 21, 23, 29 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bothra et al. in view of Bandyopadhyay et al. (US 5,814,555).

In re claims 21 and 23, Bothra et al. do not teach that the first dielectric layer comprises silicon oxide formed by PECVD.

Bandyopadhyay et al., however, in an analogous art, teach the claimed semiconductor interconnect structure, comprising:

- a substrate 10;
- a pair of conductive structures 12, wherein an air gaps 22 is disposed between the conductive structures 12; and
- a dielectric layer 20 (Fig.4) over the conductive structures 12, the dielectric layer 20 is silicon oxide formed by PECVD (col. 6, lines 1-6).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to utilize the PECVD-formed silicon oxide, as taught by Bandyopadhyay et al., as the first dielectric layer 210 in Bothra et al, since by this manner the first dielectric layer 210 (i.e. PECVD-formed silicon oxide) in Bothra et al. would have a high etching selectivity with respect to the etch stop layer 220 (i.e. silicon nitride), which, in turn, would be beneficial to the formation of the opening 224 or 226 without compromising the integrity of the conductive structure 206 or 208.

In re claim 29, Bothra et al teach that the second dielectric layer 220 is to provide the desired inter-layer dielectric thickness (col. 3, lines 44-45) but do not teach that it comprises silicon oxide.

However, silicon oxide has been widely used as the inter-layer dielectric, as evidenced by Bandyopadhyay et al. (col. 4, lines 20-21).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made to use silicon oxide, as suggested by Bandyopadhyay et al. , as the second dielectric layer in Bothra et al, since silicon oxide is a good candidate for inter-layer dielectric.

In re claim 32, the selection of the width of the opening is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). In this case, one of the ordinary skill in the art would have been motivated to choose a desired width of the opening in conjunction with a desired dimension of the air gap and the thickness of the etch stop so that the opening would not physically connected with the air gap to avoid the short-circuited between the conductive structure and the conductive material to be filled in the opening.

8. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bothra et al. in view of Ngo et al. (US 6,190,966).

Bothra et al. teach that the etch stop layer 220 is silicon nitride (col. 4, lines 39-41) over the first dielectric layer 210 but do not teach that the etch stop layer is formed by PECVD.

Ngo, however, in an analogous art, teach the etch stop layer (i.e. silicon nitride) is formed by PECVD process (abstract).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to utilize the PECVD-formed silicon nitride, as taught by Ngo. et al., as

the etch stop layer in Bothra et al., since PECVD process is a good candidate for forming etch stop materials, such as silicon nitride.

9. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bothra et al. in view of Ackermann et al. (US 5,062,508).

Bothra et al. do not teach using photo-induced CVD for forming silicon nitride.

However, Ackermann et al. suggested that using photo-induced CVD (i.e. PICVD) for forming dielectric material has the advantages of applying the dielectric coating on a variety of geometric surface, including planar, curved and large area (abstract).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to utilize the PICVD process, as suggested by Ackermann et al., for forming the etch stop layer of Bothra et al., since PICVD is a good candidate for forming the etch stop layer over the first dielectric layer, regardless of the geometry of the first dielectric layer.

Response to Arguments

10. Applicant's arguments filed 9/10/04 have been considered but are moot in view of the new ground(s) of rejection.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (8:00 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-ming Lee
Primary Examiner
Art Unit 2823

Nov. 17, 2004

HSIEN-MING LEE
PRIMARY EXAMINER